WEST Search History

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DATE: Tuesday, May 18, 2004

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L21	6249449[uref]	1
☐	L20	L19 not l11	12
☐	L19	l16 and l10	20
☐	L18	l16 same l10	1
☐	L17	L16 same l15	5
☐	L16	(clear$3 or flush$3 or eras$4) near5 data	78855
☐	L15	(memory or cache)adj5 divi$4 near6 (sub-region or sub-section or sub-block or sub-unit or sub-area or sub-divi$4)	345
☐	L11	L10 and l7	8
☐	L10	(memory or cache)adj5 divi$4 near6 (subregion or subsection or subblock or subunit or subarea or subdivi$4)	178
☐	L9	(memory or cache)adj5 divi4 near6 (subregion or subsection or subblock or subunit or subarea or subdivi$4)	0
☐	L8	L7 same l6	29
☐	L7	(clear$3 or flush$3) near5 data	48756
☐	L6	L5 or l3	5151
☐	L5	L4 or l2	4965
☐	L4	(memory or cache) near6 (subregion or subsection or subblock or subunit or subarea or subdivi$4)	3637
☐	L3	(memory or cache) near6 (subregion or subsection or subblock or subunit or subarea or sub-divi$4)	1511
☐	L2	(memory or cache) near6 (sub-region or sub-section or sub-block or sub-unit or sub-area)	1456
☐	L1	(clear$3 or flush$3) near5 (memory or cache) near6 (sub-region or sub-section or sub-block or sub-unit or sub-area)	1

END OF SEARCH HISTORY

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WEST Search History

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DATE: Tuesday, May 18, 2004

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L16	L14 and l13	3
☐	L15	L14 same l13	0
☐	L14	(clear$3 or flush$3) near3 data	36377
☐	L13	memory near5 (sub-divi$4 or subdivi$4) near6(sub-region or sub-area or sub-section or sub-block)	26
☐	L12	L11 and l8	2
☐	L11	memory near5(sub-divi$4 or subdivi$4) adj6(sub-region or sub-area or sub-section or sub-block)	24
☐	L10	L8 and l4	67
☐	L9	L8 same l4	0
☐	L8	(clear$3 or flush$3) near3 data near5 memory	3117
☐	L7	L4 and l1	1
☐	L6	L4 same l1	0
☐	L5	L4 same l4	1046
☐	L4	memory near5 (sub-region or sub-area or sub-section or sub-block)	1046
☐	L3	memory near35 (sub-region or sub-area or sub-section or sub-block)	1462
☐	L2	(clear$3 or flush$3) near3 data near5 memory adj3 sub adj1 (region or area or section or block)	0
☐	L1	(clear$3 or flush$3) near3 data near5 memory adj3 (region or area or section or block)	142

END OF SEARCH HISTORY

h e b b cg b chh e e e f ff e ch e b

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Search Results - Record(s) 1 through 5 of 5 returned.

☐ 1. Document ID: US 20020181285 A1

Using default format because multiple data bases are involved.

L17: Entry 1 of 5 File: PGPB Dec 5, 2002

PGPUB-DOCUMENT-NUMBER: 20020181285
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020181285 A1

TITLE: Nonvolatile storage system

PUBLICATION-DATE: December 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
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Ouchi, Katsumi	Higashimurayama		JP	

US-CL-CURRENT: 365/185.22

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6584014 B2

L17: Entry 2 of 5 File: USPT Jun 24, 2003

DOCUMENT-IDENTIFIER: US 6584014 B2
TITLE: Nonvolatile storage system

Brief Summary Text (28):
(4) The following will describe a nonvolatile memory related to the present invention from a further aspect. A nonvolatile storage system comprises a control unit and a plurality of nonvolatile memories. Said control unit receives data and address information from an external device to then control the storing of the data received from said external device into said plurality of nonvolatile memories, the reading out of the data thus stored in said nonvolatile memories, and the erasing of the data stored in said nonvolatile memories, while said nonvolatile memories each respond to an operation instruction from the control unit to thereby perform a write-in operation of storing data supplied from said control unit, a read-out

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operation of reading the stored data and supplying it to the control unit, and an erasure operation of erasing the stored data. The control unit then sub-divides the data received from the external device into data portions of a predetermined size and performs an interleaving operation of supplying the first nonvolatile memory with the first one of thus sub-divided data portions together with a write-in operation instruction and supplying the second nonvolatile memory with the second data portion together with a write-in operation instruction while data is being written to the first nonvolatile memory, thus sequentially supplying all of these sub-divided data portions to the plurality of nonvolatile memories. If a write-in error occurred while predetermined data is being written to any one of the plurality of nonvolatile memories, when having detected the write-in error, the control unit controls data storage in supplying said predetermined data together with a write-in operation instruction to the nonvolatile memory engaged in the write-in operation and also to other nonvolatile memories except those to which sub-divided data portions are to be written after the occurrence of the write-in error.

CLAIMS:

12. Nonvolatile storage system comprising a control unit and a plurality of nonvolatile memories, wherein: said control unit receives external data and address information to thereby control storage of said received external data to said plurality of nonvolatile memories, read-out of said external data from said nonvolatile memories, and erasure of said data stored in said nonvolatile memories; each of said nonvolatile memories responds to an operation instruction sent from said control unit to thereby perform a write-in operation of storing data supplied from said control unit, a read-out operation of reading out the stored data and then supplying said data to said controller, and an erasure operation of erasing the stored data; said control unit sub-divide said received external data into data portions of a predetermined size to then perform an interleaving operation of supplying a first data portion of the sub-divided data portions to the first nonvolatile memory together with a write-in operation instruction and then supplying a second data portion to the second nonvolatile memory together with the write-in operation instruction while writing the data to said first nonvolatile memory, thus sequentially supplying all of said sub-divided data portions to said plurality of nonvolatile memories respectively; and when having detected a write-in error which occurred during writing of predetermined data to any one of said plurality of nonvolatile memories, said control unit controls data storage of supplying said predetermined data together with the write-in operation instruction to each of the nonvolatile memories other than the nonvolatile memory currently involved in the write-in operation and the nonvolatile memories that are made subject to writing of the sub-divided data portion after the occurrence of said write-in error.

☐ 3. Document ID: US 6288941 B1

L17: Entry 3 of 5 File: USPT Sep 11, 2001

DOCUMENT-IDENTIFIER: US 6288941 B1
TITLE: Electrically erasable semiconductor non-volatile memory device having memory cell array divided into memory blocks

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Detailed Description Text (74):
In FIG. 28, the data block DB to be erased is specified by the address input signal ay. If the data block DB0 is erased, only the erase control signal 4er01 is made a high level, and the erase control signals 4er11, 4er21, 4er71 remain at a low level. In this case, the memory cell group of each divided sub-block SB includes Q1 to Q4 connected to the data line D1 of the data block DB0, Q5 to Q8 connected to the data line D2, and Q9 to Q12 connected to the data line Dm. In FIG. 28, while the memory cell group connected to one data line D is treated as the divided sub-block and connected to the information erase signal generation circuit ERC01 to ERC7k, several memory cell groups connected to two or more data lines D may be treated as the divided sub-block DB.

☐ 4. Document ID: US 5761119 A

L17: Entry 4 of 5 File: USPT Jun 2, 1998

DOCUMENT-IDENTIFIER: US 5761119 A
TITLE: Nonvolatile semiconductor memory with a plurality of erase decoders connected to erase gates

Brief Summary Text (26):
However, with collective erase, data not desired to be erased is forced to be erased. In this case, the collective erase is not useful and is associated with various difficulties. In order to solve this problem, it may be considered that the memory cell area is divided into a plurality of small sub-areas (hereinafter called blocks) and data is erased on the block unit basis (hereinafter called block erase). In more particular, erase gates of memory cells connected to two word lines are coupled together. In erasing data, one of a plurality of such common erase lines is selected and applied with an erase voltage V.sub.EG =20 V by means of an erase decoder (not shown). In this manner, only memory cells belonging to the selected block can be erased, thus allowing block erase.

☐ 5. Document ID: US 5418742 A

L17: Entry 5 of 5 File: USPT May 23, 1995

DOCUMENT-IDENTIFIER: US 5418742 A
TITLE: Nonvolatile semiconductor memory with block erase select means

Brief Summary Text (26):
However, with a collective erase, data not desired to be erased nevertheless forced to be erased. In this case, the collective erase is not useful and is associated with various difficulties. In order to solve this problem, it may be considered that the memory cell area is divided into a plurality of small sub-areas

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(hereinafter called blocks) and data is erased on the block unit basis (hereinafter called block erase). In more particular, erase gates of memory cells connected to two word lines are coupled together. In erasing data, one of a plurality of such common erase lines is selected and applied with an erase voltage V.sub.EG =20 V by means of an erase decoder (not shown). In this manner, only memory cells belonging to the selected block can be erased, thus allowing block erase.

Terms	Documents
L16 same L15	5

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